CLAIMS

Please amend the claims as follows:

1. (currently amended) A method of specifying a trace array for a simulation model of an electronic design in a data processing system, said method comprising:

permitting a user to specify ~~specifying~~ one or more design entities within a simulation model with one or more statements in one or more hardware description language (HDL) files, wherein specifying the one or more design entities includes specifying a plurality of signals, functional logic, and any storage elements that define functional operation of the electronic design;

permitting a user to specify, in one or more statements in the one or more HDL files, ~~specifying~~ an instrumentation entity that monitors at least one design entity among the one or more design entities but does not contribute to functional operation of the electronic design, wherein specifying the instrumentation entity includes specifying a trace array ~~for storing trace data that will be generated through simulation~~ within the instrumentation entity and indicating a monitored signal set including at least one signal among the plurality of signals, wherein the trace array concurrently stores multiple values for the monitored signal set obtained over multiple cycles of functional operation of the simulation model; and

storing said one or more HDL files.

2. (currently amended) The method of Claim 1, wherein said specifying a trace array comprises specifying a ~~set of~~ control signal[[s]] among said plurality of signals, wherein a ~~for which~~ value[[s]] ~~are to be presented~~ of said monitored signal set is stored within the trace array only on those cycles of functional operation during which the control signal is asserted.

3. (currently amended) The method of Claim 1 [[2]], wherein specifying a trace array comprises specifying an association between an enumerated value and a ~~set of~~ value[[s]] of the at least one signal comprising said monitored signal[[s]] set.

4. (currently amended) The method of Claim 1, wherein said specifying said trace array comprises specifying a particular type for the trace array among a plurality of different types of trace arrays ~~said trace array in one or more statements within an HDL file declaring an instrumentation entity containing the trace array~~.

5. (currently amended) The method of Claim 1, wherein said specifying said trace array comprises specifying said trace array ~~comprises specifying said trace array~~ within an HDL file declaring a design entity.

6. (currently amended) A method of preparing a simulation model of an electronic ~~digital~~ design within a data processing system, said method comprising:

receiving one or more hardware description language (HDL) files declaring a plurality of design entities forming the electronic ~~digital~~ design, wherein the plurality of design entities includes a plurality of signals, functional logic, and any storage elements that define functional operation of the electronic design, wherein said one or more HDL files further include one or more statements specifying an instrumentation entity that monitors at least one design entity among the one or more design entities but does not contribute to functional operation of the electronic design, specifying a trace array ~~for storing trace data generated through simulation~~ within the instrumentation entity, and indicating a monitored signal set including at least one signal among the plurality of signals ~~of the simulation model~~; and

in response to receipt of the one or more HDL files, parsing and processing said one or more HDL files to generate a simulation model formed of representations of instances of the plurality of the design entities and a trace array within at least one of the instances of the plurality of design entities, wherein the trace array is configured to concurrently store multiple values for the monitored signal set obtained over multiple cycles of functional operation of the simulation model; and

placing the simulation model in data storage.

7. (currently amended) The method of Claim 6, wherein said parsing and processing said one or more HDL files includes creating, within the trace array, storage for multiple values of ~~a set of~~ the monitored signal[[s]] set.

8. (currently amended) The method of Claim 7, wherein said parsing and processing said one or more HDL files includes creating an association between an enumerated value and a ~~set of~~ value[[s]] of the at least one signal comprising said monitored signal[[s]] set.

9. (currently amended) The method of Claim 6, wherein said receiving one or more HDL files comprises receiving an HDL file including one or more statements declaring a particular type for said trace array among a plurality of different types of trace arrays ~~an instrumentation entity containing the trace array~~.

10. (original) The method of Claim 6, said receiving one or more HDL files comprises receiving an HDL file including one or more statements declaring a design entity containing the trace array.

11. (original) The method of Claim 6, wherein said parsing and processing includes automatically replicating said trace array within a plurality of instances of an entity declared by an HDL file containing the one or more statements specifying the trace array.

12. (currently amended) A method of reporting simulation data obtained by the simulation of an ~~digital~~ electronic design within a data processing system, said method comprising:

a simulator running a testcase against a simulation model of the electronic design, wherein:

the simulation model is formed of representations of instances of a ~~the~~ plurality of ~~the~~ design entities,

the instances of the design entities contain a plurality of signals, functional logic, and any storage elements that define functional operation of the electronic design, ~~and~~

each instance of at least a particular design entity of the plurality of design entities contains an instance of an instrumentation entity that monitors the containing instance of the particular design entity but does not contribute to functional operation of the electronic design, and

each instance of the instrumentation entity contains a trace array logically coupled to receive a monitored signal set including at least one signal among the plurality of signals ~~within one of the plurality of design entities~~;

recording trace data for the monitored signal set within the trace array during the running of the testcase ~~said simulation~~, wherein the recording includes concurrently storing within the trace array multiple values of the monitored signal set obtained over multiple cycles of functional operation of the simulation model; and

exporting said trace data from said trace array in a trace file and storing said trace file in data storage.

13. (currently amended) The method of Claim 12, wherein the trace array is further logically coupled to receive a control signal among the plurality of signals, and wherein recording trace data includes recording, within the trace array, values assumed by the monitored ~~a set of~~ signal[[s]] set during only those cycles of functional operation during which the control signal is asserted ~~simulation~~.

14. (currently amended) The method of Claim 13, wherein exporting the trace data in a trace file includes exporting the trace data in a trace file indicating an association between an enumerated value and a ~~set of~~ value[[s]] of said monitored signal[[s]] set.

15. (canceled)

16. (currently amended) A data processing system, comprising:

means for specifying one or more design entities within a simulation model of an electronic design with one or more statements in one or more hardware description language (HDL) files, wherein the means for specifying the one or more design entities includes means for specifying a plurality of signals, functional logic, and any storage elements that define functional operation of the electronic design;

means for specifying, in one or more statements in the one or more HDL files, an instrumentation entity that monitors at least one design entity among the one or more design entities but does not contribute to functional operation of the electronic design, wherein the

means for specifying the instrumentation entity includes means for specifying a trace array ~~for storing data generated through simulation~~ within the instrumentation entity and indicating a monitored signal set including at least one signal among the plurality of signals, wherein the trace array concurrently stores multiple values for the monitored signal set obtained over multiple cycles of functional operation of the simulation model ; and

means for storing said one or more HDL files.

17. (currently amended) The data processing system of Claim 16, wherein said means for specifying a trace array comprises means for specifying a ~~set of~~ control signal[[s]] among said plurality of signals, wherein a ~~for which~~ value[[s]] ~~are to be presented~~ of said monitored signal set is stored within the trace array only on those cycles of functional operation during which the control signal is asserted.

18. (currently amended) The data processing system of Claim 16, wherein said means for specifying a trace array comprises means for specifying an association between an enumerated value and a ~~set of~~ value[[s]] of the at least one signal comprising said monitored signal[[s]] set.

19. (currently amended) The data processing system of Claim 16, wherein said means for specifying said trace array comprises means for specifying, for said trace array, a particular type among a plurality of different types of trace arrays ~~in one or more statements within an HDL file declaring an instrumentation entity containing the trace array~~.

20. (original) The data processing system of Claim 16, wherein said means for specifying said trace array comprises means for specifying said trace array within an HDL file declaring a design entity.

21. (currently amended) A data processing system for preparing a simulation model of an electronic ~~digital~~ design, said data processing system comprising:

means for receiving one or more hardware description language HDL files declaring a plurality of design entities forming the digital design, wherein the plurality of design entities includes a plurality of signals, functional logic, and any storage elements that define functional

operation of the electronic design, wherein said one or more HDL files further include one or more statements specifying an instrumentation entity that monitors at least one design entity among the one or more design entities but does not contribute to functional operation of the electronic design, specifying a trace array ~~for storing trace data generated through simulation~~ within the instrumentation entity, and indicating a monitored signal set including at least one signal among the plurality of signals ~~of the simulation model~~; and

means, responsive to receipt of the one or more HDL files, for parsing and processing said one or more HDL files to generate a simulation model formed of representations of instances of the plurality of the design entities and a trace array within at least one of the instances of the plurality of design entities, wherein the trace array concurrently stores multiple values for the monitored signal set obtained over multiple cycles of functional operation of the simulation model.

22. (currently amended) The data processing system of Claim 21, wherein said means for parsing and processing said one or more HDL files includes means for creating, within the trace array, storage for multiple values of ~~a set of~~ the monitored signal[[s]] set.

23. (currently amended) The data processing system of Claim 22, wherein said means for parsing and processing said one or more HDL files includes means for creating an association between an enumerated value and a ~~set of~~ value[[s]] of the at least one signal comprising said monitored signal[[s]] set.

24. (currently amended) The data processing system of Claim 21, wherein said means for receiving one or more HDL files comprises means for receiving an HDL file including one or more one or more statements declaring a particular type for said trace array among a plurality of different types of trace arrays ~~an instrumentation entity containing the trace array~~.

25. (original) The data processing system of Claim 21, said means for receiving one or more HDL files comprises means for receiving an HDL file including one or more statements declaring a design entity containing the trace array.

26. (original) The data processing system of Claim 21, wherein said means for parsing and processing includes means for automatically replicating said trace array within a plurality of instances of an entity declared by an HDL containing the one or more statements specifying the trace array.

27. (currently amended) A data processing system, ~~said data processing system~~ comprising:

means for running a testcase against a simulation model of an electronic design, wherein:

the simulation model is formed of representations of instances of a ~~the~~ plurality of ~~the~~ design entities, ~~and~~

the instances of the design entities contain a plurality of signals, functional logic, and any storage elements that define functional operation of the electronic design,

each instance of at least a particular design entity of the plurality of design entities contains an instance of an instrumentation entity that monitors the containing instance of the particular design entity but does not contribute to functional operation of the electronic design, and

each instance of the instrumentation entity contains a trace array logically coupled to receive a monitored signal set including at least one signal among the plurality of signals ~~within one of the plurality of design entities~~;

means for recording trace data for the monitored signal set within the trace array during the running of the testcase, wherein the recording includes concurrently storing within the trace array multiple values of the monitored signal set obtained over multiple cycles of functional operation of the simulation model ~~said simulation~~; and

means for exporting said trace data from said trace array in a trace file and storing said trace file in data storage.

28. (currently amended) The data processing system of Claim 27, wherein the trace array is further logically coupled to receive a control signal among the plurality of signals, and wherein the means for recording trace data includes means for recording, within the trace array, values assumed by ~~a set of~~ the monitored signal[[s]] set during only those cycles of functional operation during which the control signal is asserted ~~simulation~~.

29. (original) The data processing system of Claim 27, wherein said means for exporting the trace data in a trace file includes means for exporting the trace data in a trace file indicating an association between an enumerated value and a ~~set of~~ value[[s]] of said monitored signal[[s]] set.

30. (canceled)

31. (currently amended) An apparatus ~~program product,~~ comprising a tangible computer usable medium containing program code, said program code including:

means for specifying one or more design entities within a simulation model of an electronic design with one or more statements in one or more hardware description language (HDL) files, wherein the means for specifying the one or more design entities includes means for specifying a plurality of signals, functional logic, and any storage elements that define functional operation of the electronic design;

means for specifying, in one or more statements in the one or more HDL files, an instrumentation entity that monitors at least one design entity among the one or more design entities but does not contribute to functional operation of the electronic design, wherein the means for specifying the instrumentation entity includes means for specifying a trace array ~~for storing adapt generated through simulation~~ within the instrumentation entity and for indicating a monitored signal set including at least one signal among the plurality of signals, wherein the trace array concurrently stores multiple values for the monitored signal set obtained over multiple cycles of functional operation of the simulation model; and

means for storing said one or more HDL files.

32. (currently amended) The apparatus ~~program product~~ of Claim 31, wherein said means for specifying a trace array comprises means for specifying a ~~set of~~ control signal[[s]] among said plurality of signals, wherein a ~~for which~~ value[[s]] ~~are to be presented~~ of said monitored signal set is stored within the trace array only on those cycles of functional operation during which the control signal is asserted.

33. (currently amended) The apparatus ~~program product~~ of Claim 31, wherein said means for specifying a trace array comprises means for specifying an association between an enumerated value and a ~~set of~~ value[[s]] of the at least one signal comprising said monitored signal[[s]] set.

34. (currently amended) The apparatus ~~program product~~ of Claim 31, wherein said means for specifying said trace array comprises means for specifying, for said trace array, a particular type among a plurality of different types of trace arrays ~~in one or more statements within an HDL file declaring an instrumentation entity containing the trace array~~.

35. (currently amended) The apparatus ~~program product~~ of Claim 31, wherein said means for specifying said trace array comprises means for specifying said trace array within an HDL file declaring a design entity.

36. (currently amended) An apparatus ~~program product~~ for preparing a simulation model of an electronic ~~digital~~ design, said apparatus ~~program product~~ comprising a tangible computer usable medium containing program code, said program code including:

means for receiving one or more hardware description language (HDL) files declaring a plurality of design entities forming the electronic ~~digital~~ design, wherein the plurality of design entities includes a plurality of signals, functional logic, and any storage elements that define functional operation of the electronic design, wherein said one or more HDL files further include one or more statements specifying an instrumentation entity that monitors at least one design entity among the one or more design entities but does not contribute to functional operation of the electronic design, specifying a trace array ~~for storing trace data generated through simulation~~ within the instrumentation entity, and indicating a monitored signal set including at least one signal among the plurality of signals ~~of the simulation model~~; and

means, responsive to receipt of the one or more HDL files, for parsing and processing said one or more HDL files to generate a simulation model formed of representations of instances of the plurality of the design entities and a trace array within at least one of the instances of the plurality of design entities, wherein the trace array concurrently stores multiple values for the monitored signal set obtained over multiple cycles of functional operation of the simulation model.

37. (currently amended) The apparatus ~~program product~~ of Claim 36, wherein said means for parsing and processing said one or more HDL files includes means for creating, within the trace array, storage for multiple values of ~~a set of~~ the monitored signal[[s]] set.

38. (currently amended) The apparatus ~~program product~~ of Claim 37, wherein said means for parsing and processing said one or more HDL files includes means for creating an association between an enumerated value and a ~~set of~~ value[[s]] of said monitored signal[[s]] set.

39. (currently amended) The apparatus ~~program product~~ of Claim 36, wherein said means for receiving one or more HDL files comprises means for receiving an HDL file including one or more statements declaring a particular type for said trace array among a plurality of different types of trace arrays ~~an instrumentation entity containing the trace array~~.

40. (currently amended) The apparatus ~~program product~~ of Claim 36, said means for receiving one or more HDL files comprises means for receiving an HDL file including one or more statements declaring a design entity containing the trace array.

41. (currently amended) The apparatus ~~program product~~ of Claim 36, wherein said means for parsing and processing includes means for automatically replicating said trace array within a plurality of instances of an entity declared by an HDL file containing the one or more statements specifying the trace array.

42. (currently amended) An apparatus ~~program product~~ comprising a computer usable medium containing program code, said program code including:

means for running a testcase against a simulation model of an electronic design, wherein:

the simulation model is formed of representations of instances of a ~~the~~ plurality of ~~the~~ design entities, ~~and~~

the instances of the design entities contain a plurality of signals, functional logic, and any storage elements that define functional operation of the electronic design,

each instance of at least a particular design entity of the plurality of design entities contains an instance of an instrumentation entity that monitors the containing instance of the particular design entity but does not contribute to functional operation of the electronic design, and

each instance of the instrumentation entity contains a trace array logically coupled to receive a monitored signal set including at least one signal among the plurality of signals ~~within one of the plurality of design entities~~; and

means for recording trace data for the monitored signal set within the trace array during the running of the testcase, wherein the recording includes concurrently storing within the trace array multiple values of the monitored signal set obtained over multiple cycles of functional operation of the simulation model ~~said simulation~~; and

means for exporting said trace data from said trace array in a trace file and storing said trace file in data storage.

43. (currently amended) The apparatus ~~program product~~ of Claim 42, wherein the trace array is further logically coupled to receive a control signal among the plurality of signals, and wherein the means for recording trace data includes means for recording, within the trace array, values assumed by ~~a set of~~ the monitored signal[[s]] set during only those cycles of functional operation during which the control signal is asserted ~~simulation~~.

44. (currently amended) The apparatus ~~program product~~ of Claim 42, wherein said means for exporting the trace data in a trace file includes means for exporting the trace data in a trace file indicating an association between an enumerated value and a ~~set of~~ value[[s]] of said monitored signal[[s]] set.

45. (canceled)